DISCOVERY

vs

Current IIGS

ERS

The following is a list of the changes from the current IIgs to the DISCOVERY, and they are divided into groups depending on the scope of the change:

FUNCTIONAL

• The Base system RAM has changed from banks $00,01,E0 & E1 to banks $00-0F,E0 & E1. This means that the memory expansion card will start at bank $10 and continue up through bank $7F. If any third party memory expansion cards are decoding addresses they may not work properly.

• The base ROM has changed from banks $FE & FF to $FC-FF. This means that the memory expansion card CROMSEL.L signal will be active only from banks $F0-FB.

• Text pages 1,1x were not able to be shadowed in the FPI. The CYA powers-up with text pages 1,1x shadowing enabled, this shadowed area can be inhibited if the shadow register ($C035) bit 0 is set to a 1.

• The current IIGS depends on the dynamic RAM discharging (losing the current data) when the power is turned off to determine if the system is in a cold start or a warm start. The CYA has a POC (power on clear) bit that gets set to a 1 on power-up but is not changed if a reset occurs. The POC bit is in the CYA register ($C036) bit 6.

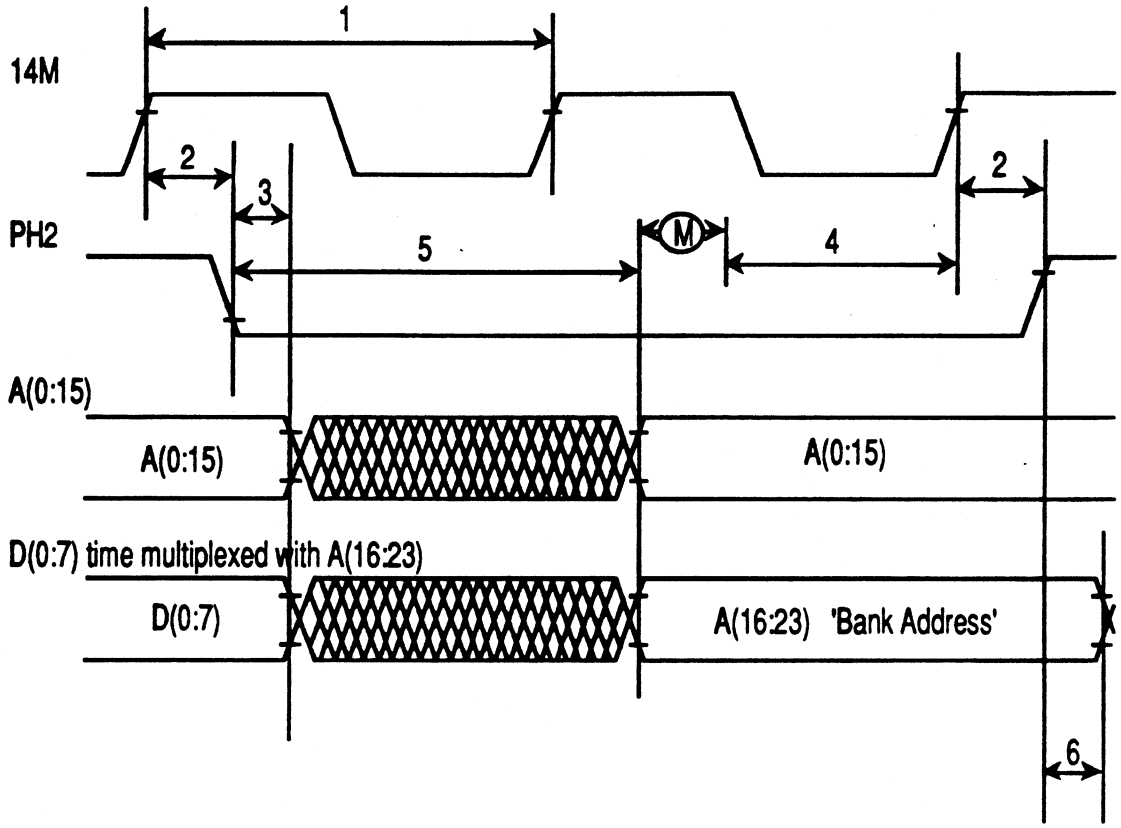
REMOVAL OF NON-USED FEATURE

• The ROMBANK soft switch functionality has been removed due to the fact that the firmware did not support it (if the bank was switched in the system would crash).

ADDITION OF REQUESTED FEATURE

• A two pin Molex connector has been added to an input pin, P36, of the keyboard μ-processor. When there is a jumper installed the firmware will prohibit access to the control panel.

TIMING



ITEM	DESCRIPTION	MIN	MAX
1	CYA master clock period	70ns	
2	14M to PH2 delay		15ns
3	A(0:15) and D(0:7) hold	10ns	
4	Internal CYA A(0:23) setup		40ns
5	PH2 to A(0:23) delay		70ns
6	A(16:23) hold	10ns	
M	System Margin	15ns	

Note:

The Internal CYA A(0:23) setup of 40ns Max. is longer than the equivalent Internal FPI setup of 25ns Max. by 15ns. This forced the PH2 to A(0:23) delay to be pulled in from the standard 65C816 4Mhz Spec. (tBAS = 90ns Max. & tADS=75ns Max.) by 20ns & 5ns respectively to allow a sufficient system timing margin.

Any processor replacement in the DISCOVERY system needs to allow for this timing difference from the current IIgs to work properly.